DATA SHEET

SA5212A
Transimpedance amplifier (140MHz)

Product specification
Replaces datasheet NE/SA/SE5212A of 1995 Apr 26
IC19 Data Handbook

1998 Oct 07

Philips
Semiconductors

PHILIPS

Transimpedance amplifier (140MHz) SA5212A

DESCRIPTION

The SA5212A is a 14kΩ transimpedance, wideband, low noise differential output amplifier, particularly suitable for signal recovery in fiber optic receivers and in any other applications where very low signal levels obtained from high-impedance sources need to be amplified.

PIN CONFIGURATION

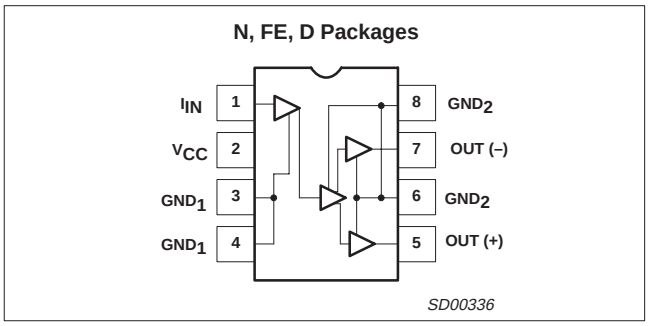


Figure 1. Pin Configuration

FEATURES

- Extremely low noise: 2.5pA/√Hz
- Single 5V supply
- Large bandwidth: 140MHz
- Differential outputs
- Low input/output impedances
- 14kΩ differential transresistance
- ESD hardened

APPLICATIONS

- Fiber-optic receivers, analog and digital
- Current-to-voltage converters
- Wideband gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA5212AD	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA5212AN	SOT97-1
8-Pin Ceramic Dual In-Line Package (DIP)	-40°C to +85°C	SA5212AFE	0580A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	SA5212A	UNIT
V_{CC}	Power Supply	6	V
$P_{D\ MAX}$	Power dissipation, T_A=25°C (still air)[1]		
	8-Pin Plastic DIP	1100	mW
	8-Pin Plastic SO	750	mW
	8-Pin Cerdip	750	mw
$I_{IN\ MAX}$	Maximum input current[2]	5	mA
T_A	Operating ambient temperature range	-40 to 85	°C
T_J	Operating junction	-55 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	°C

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance:
   8-Pin Plastic DIP: 110°C/W
   8-Pin Plastic SO: 160°C/W
   8-Pin Cerdip: 165°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode, is recommended

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	4.5 to 5.5	V
T_A	Ambient temperature ranges	-40 to +85	°C
T_J	Junction temperature ranges	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

Minimum and Maximum limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data applies at V_{CC}=5V and T_A=25°C[1].

SYMBOL	PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
V_{IN}	Input bias voltage		0.55	0.8	1.05	V
$V_{O\pm}$	Output bias voltage		2.5	3.3	3.8	V
V_{OS}	Output offset voltage				120	mV
I_{CC}	Supply current		20	26	33	mA
I_{OMAX}	Output sink/source current		3	4		mA
I_{IN}	Maximum input current (2% linearity)	Test Circuit 6, Procedure 2	±40	±80		µA
$I_{N\ MAX}$	Maximum input current overload threshold	Test Circuit 6, Procedure 4	±60	±120		µA

NOTES:

1. As in all high frequency circuits, a supply bypass capacitor should be located as close to the part as possible.

AC ELECTRICAL CHARACTERISTICS

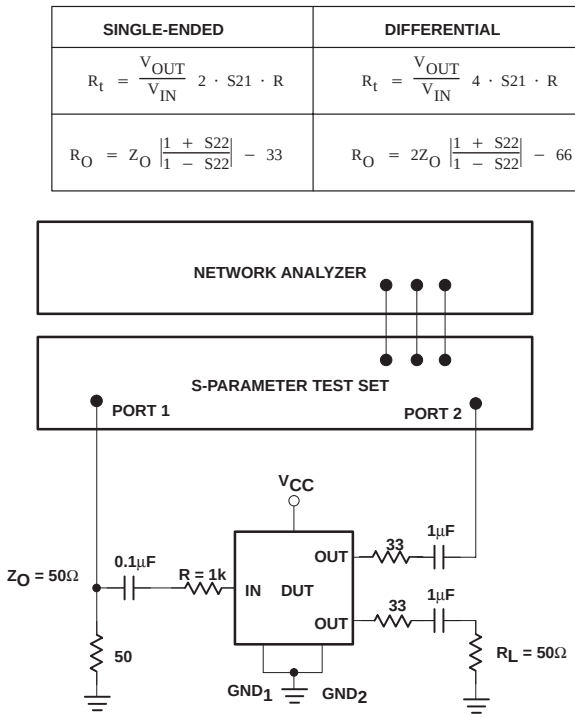
Minimum and Maximum limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data applies at V_{CC}=5V and T_A=25°C[5].

SYMBOL	PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$ Test Circuit 6, Procedure 1	9.0	14	19	kΩ
R_O	Output resistance (differential output)	DC tested	14	30	46	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	4.5	7	9.5	kΩ
R_O	Output resistance (single-ended output)	DC tested	7	15	23	Ω
f_{3dB}	Bandwidth (-3dB)	Test Circuit 1 D package, T_A = 25°C N, FE packages, T_A = 25°C	100 100	140 120		MHz
R_{IN}	Input resistance		70	110	150	Ω
C_{IN}	Input capacitance			10	18	pF
ΔR/ΔV	Transresistance power supply sensitivity	V_{CC} = 5 ±0.5V		9.6		%/V
ΔR/ΔT	Transresistance ambient temperature sensitivity	D package $\Delta T_A = T_{A\ MAX} - T_{A\ MIN}$		0.05		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		2.5		pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input) C_S = 0[1]	T_A = 25°C Test Circuit 2 Δf = 50MHz		20		nA
		Δf = 100MHz		27		
		Δf = 200MHz		40		
	C_S = 1pF	Δf = 50MHz		22		
		Δf = 100MHz		32		
		Δf = 200MHz		52		
PSRR	Power supply rejection ratio[2]	Any package DC tested ΔV_{CC} = 0.1V Equivalent AC Test Circuit 3	20	33		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	Any package f = 0.1MHz[1] Test Circuit 4		23		dB
$V_{O\ MAX}$	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 6, Procedure 3	1.7	3.2		V_{P-P}
$V_{IN\ MAX}$	Maximum input amplitude for output duty cycle of 50 ±5%[3]	Test Circuit 5		325		mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 5		2.0		ns

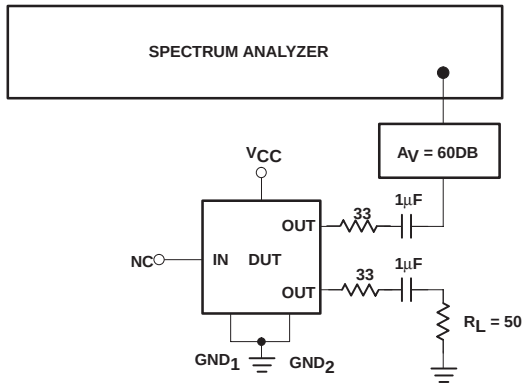
NOTES:
1. Package parasitic capacitance amounts to about 0.2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and over load tests.
4. t_R defined as 20-80% rise time. It is guaranteed by -3dB bandwidth test.
5. As in all high frequency circuits, a supply bypass capacitor should be located as close to the part as possible.

TEST CIRCUITS

SINGLE-ENDED	DIFFERENTIAL
$R_t = \frac{V_{OUT}}{V_{IN}} 2 \cdot S21 \cdot R$	$R_t = \frac{V_{OUT}}{V_{IN}} 4 \cdot S21 \cdot R$
$R_O = Z_O \left\lvert\frac{1 + S22}{1 - S22}\right\rvert - 33$	$R_O = 2Z_O \left\lvert\frac{1 + S22}{1 - S22}\right\rvert - 66$



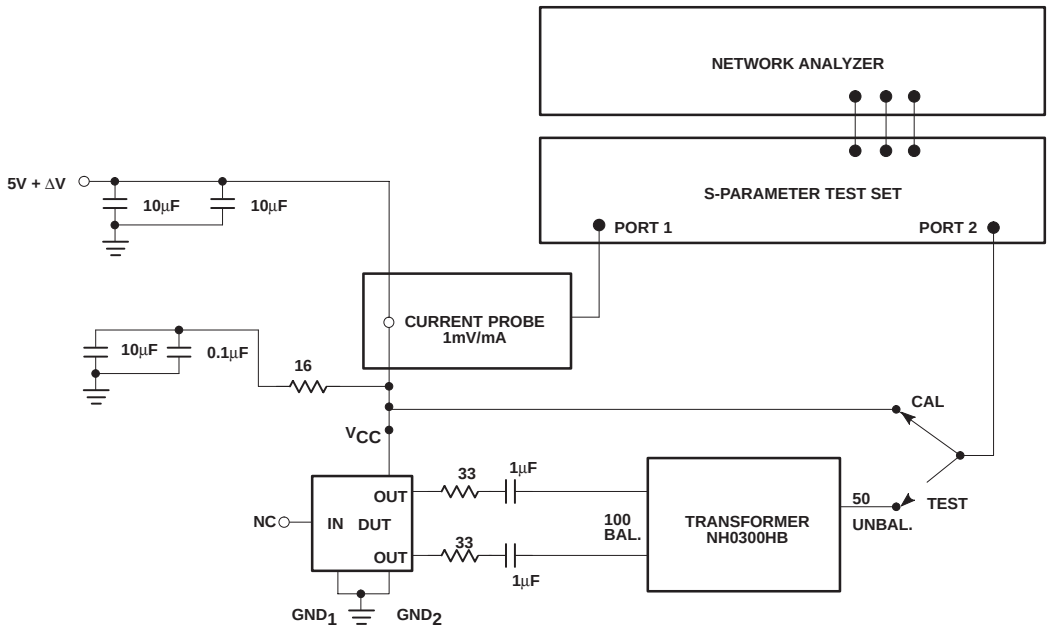
Test Circuit 1



Test Circuit 2

SD00337

Figure 2. Test Circuits 1 and 2

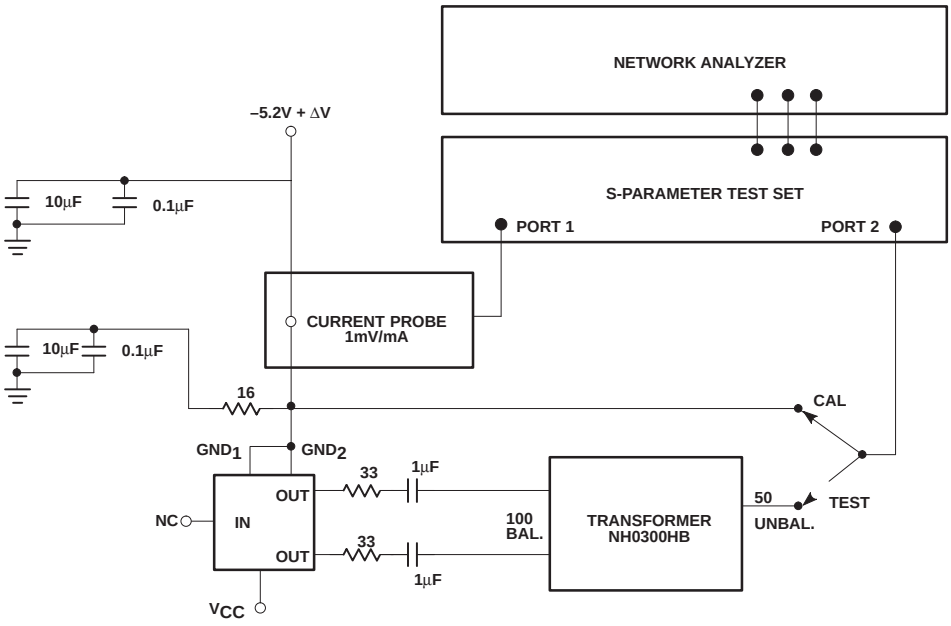


Test Circuit 3

SD00338

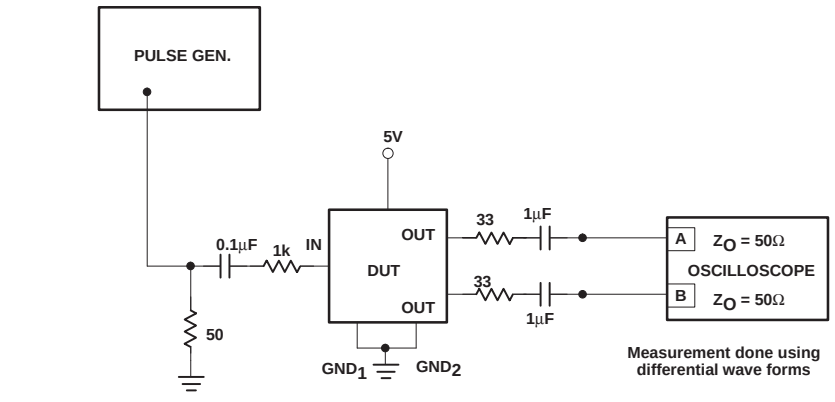
Figure 3. Test Circuit 3

TEST CIRCUITS (Continued)



Test Circuit 4 SD00339

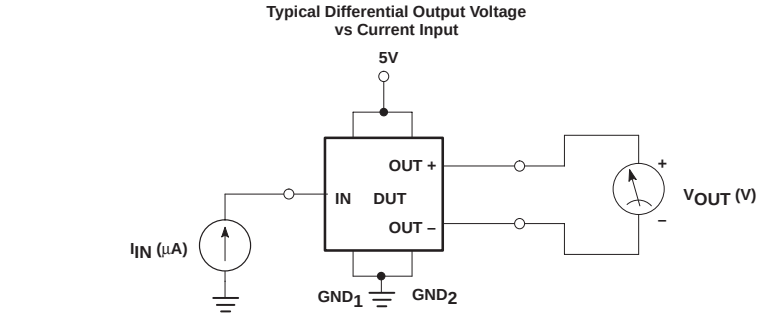
Figure 4. Test Circuit 4

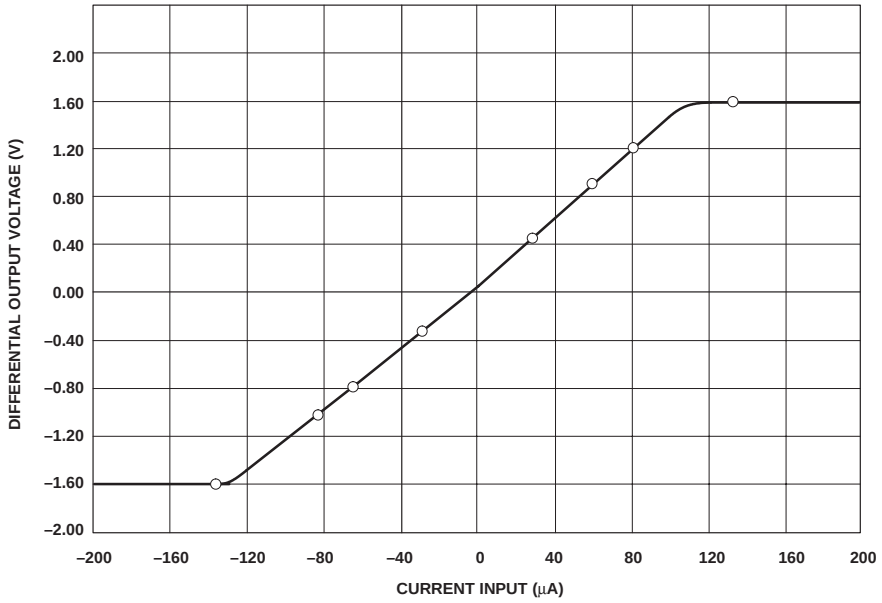


Test Circuit 5 SD00545

Figure 5. Test Circuit 5

TEST CIRCUITS (Continued)





NE5212A TEST CONDITIONS

Procedure 1

R_T measured at 30μA

$R_T = (V_{O1} - V_{O2})/(+30\mu A - (-30\mu A))$

Where: V_{O1} Measured at I_{IN} = +30μA

V_{O2} Measured at I_{IN} = –30μA

Procedure 2

Linearity = $1 - ABS((V_{OA} - V_{OB}) / (V_{O3} - V_{O4}))$

Where: V_{O3} Measured at I_{IN} = +60μA

V_{O4} Measured at I_{IN} = –60μA

$V_{OA} = R_T \cdot (+ 60\mu A) + V_{OB}$

$V_{OB} = R_T \cdot (- 60\mu A) + V_{OB}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$

Where: V_{O7} Measured at I_{IN} = +130μA

V_{O8} Measured at I_{IN} = –130μA

Procedure 4

I_{IN} Test Pass Conditions:

$V_{O7} - V_{O5} > 20mV$ and $V_{06} - V_{O5} > 20mV$

Where: V_{O5} Measured at I_{IN} = +800μA

V_{O6} Measured at I_{IN} = –80μA

V_{O7} Measured at I_{IN} = +130μA

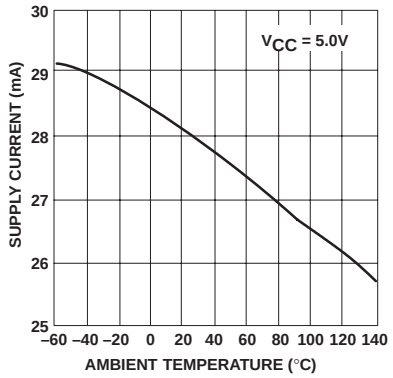
V_{O8} Measured at I_{IN} = –130μA

Test Circuit 8 *SD00340*

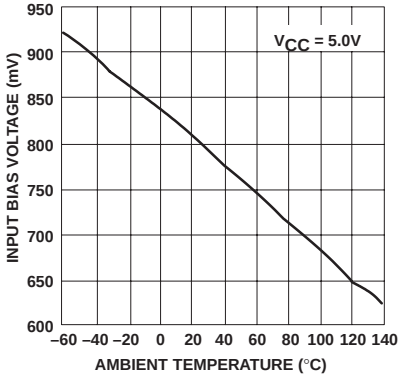
Figure 6. Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS

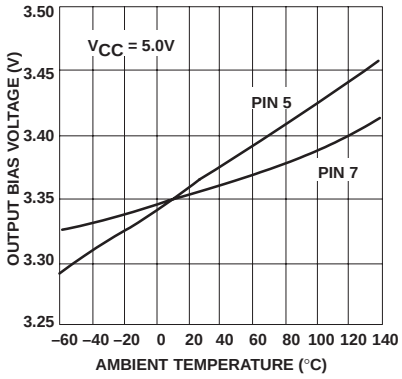
NE5212A Supply Current vs Temperature



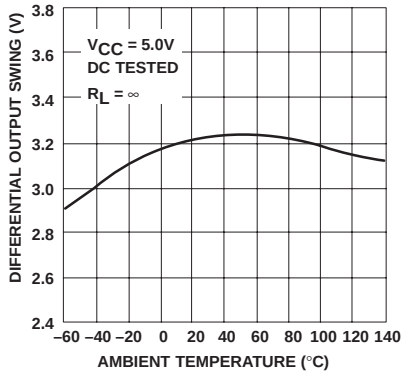
NE5212A Input Bias Voltage vs Temperature



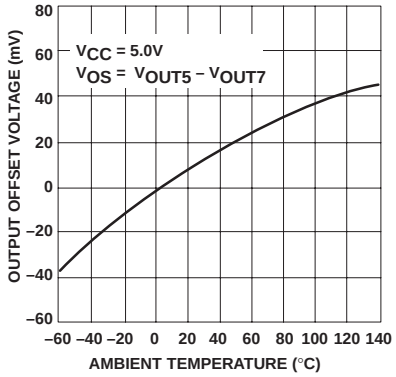
NE5212A Output Bias Voltage vs Temperature



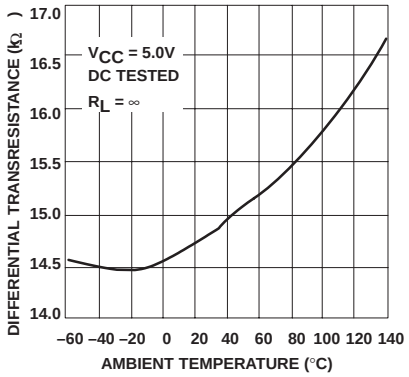
NE5212A Differential Output Swing vs Temperature



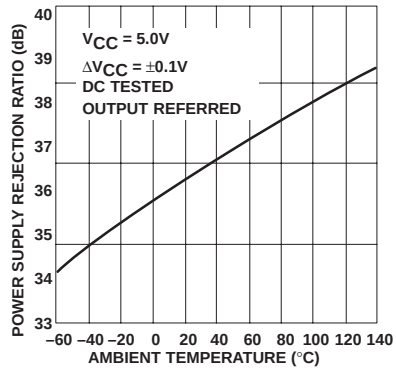
NE5212A Output Offset Voltage vs Temperature



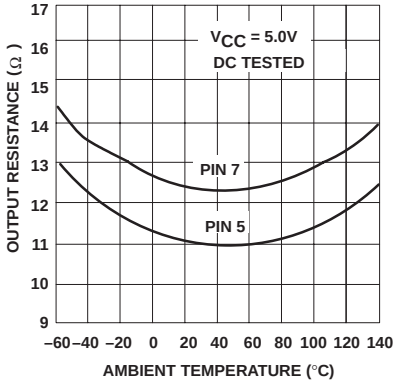
NE5212A Differential Transresistance vs Temperature



NE5212A Power Supply Rejection Ratio vs Temperature



NE5212A Output Resistance vs Temperature



NE5212A Typical Bandwidth Distribution (75 Parts from 3 Wafer Lots)

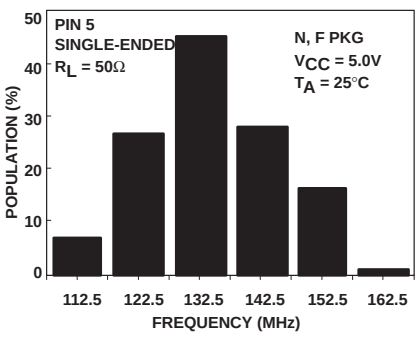


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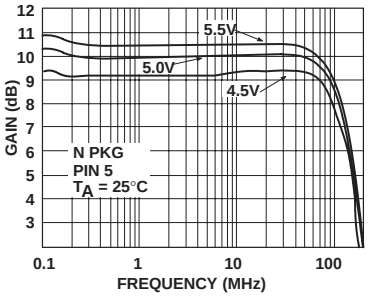
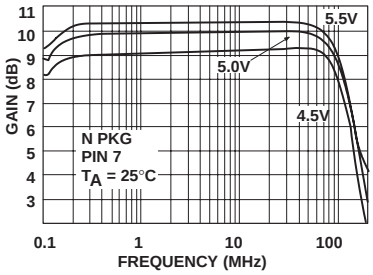
Figure 7. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

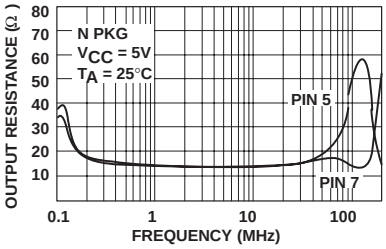
Gain vs Frequency



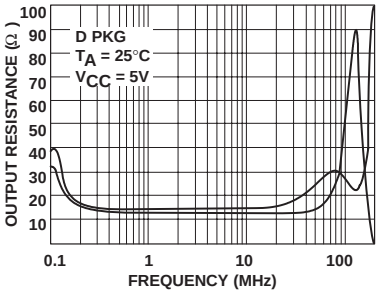
Gain vs Frequency



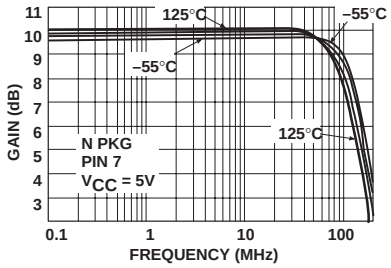
Output Resistance vs Frequency



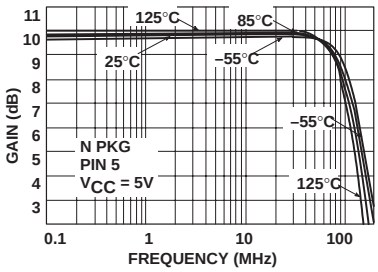
Output Resistance vs Frequency



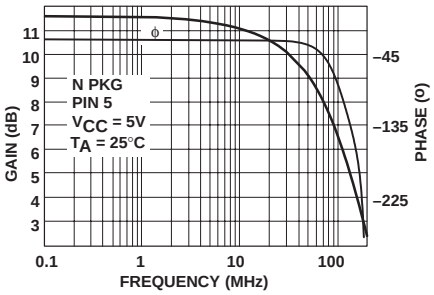
Gain vs Frequency



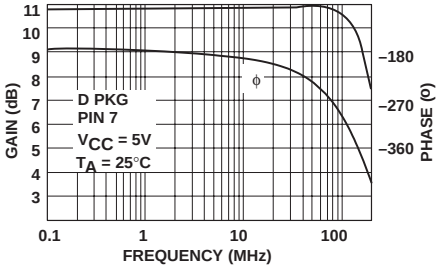
Gain vs Frequency



Gain and Phase Shift vs Frequency



Gain and Phase Shift vs Frequency



Gain and Phase Shift vs Frequency

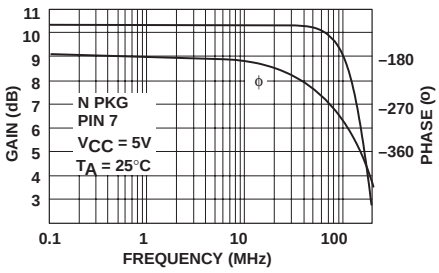


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Figure 8. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

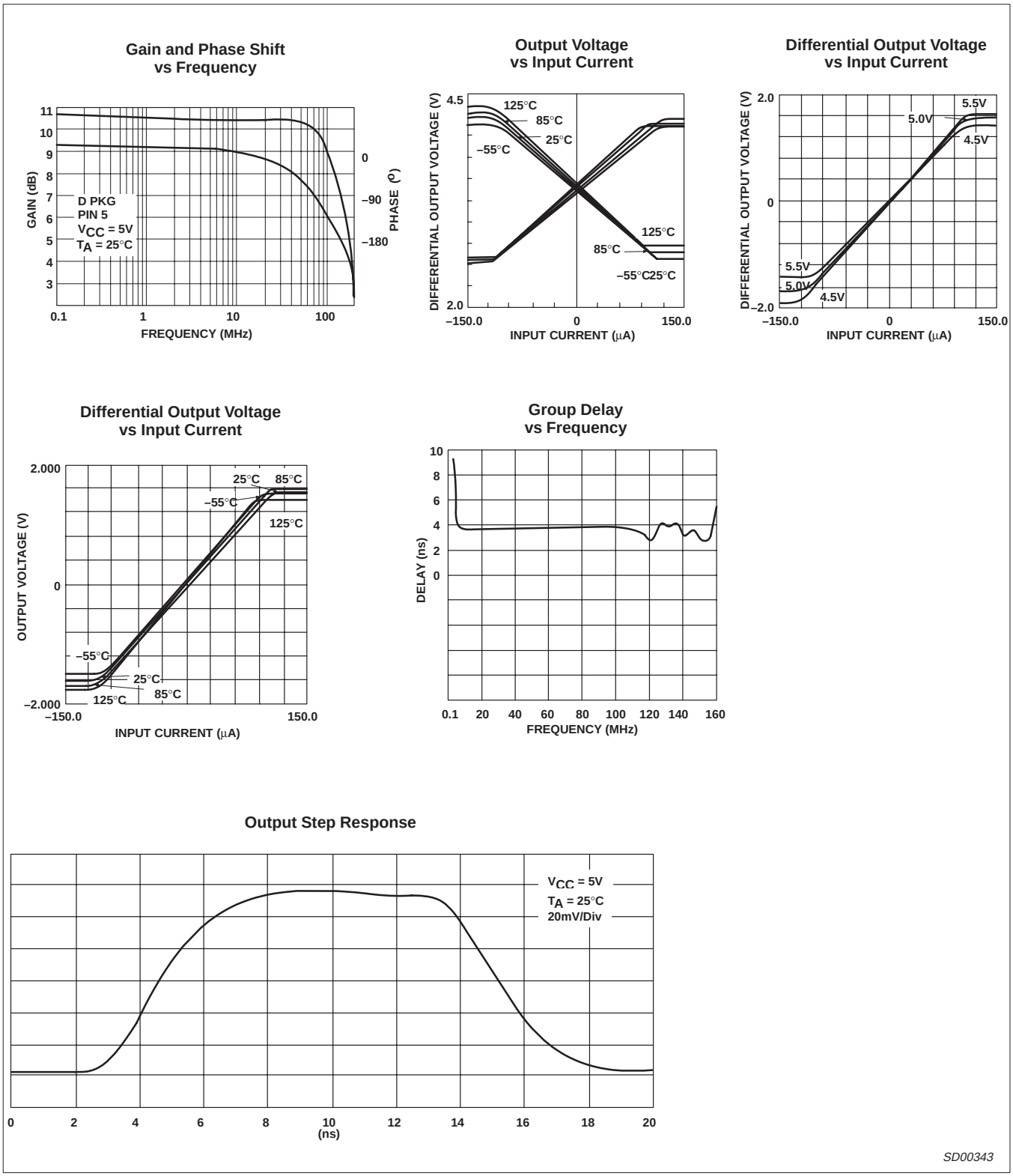


Figure 9. Typical Performance Characteristics (cont.)

THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The SA5212A is a wide bandwidth (typically 140MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 240μA. The SA5212A is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 10. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F=7kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT}(diff)}{I_{IN}} = 2R_F = 2(7.2K) = 14.4k\Omega$$

The single-ended transresistance of the amplifier is typically 7.2kΩ.

The simplified schematic in Figure 11 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, A_{VOL}≈70. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15} – Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11} – Q_{12} which are biased by constant current sources. The collectors of Q_{11} – Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 12, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that C_S=0 where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{7.2K}{70} = 103\Omega$$

More exact calculations would yield a higher value of 110Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Assuming typical values for R_F = 7.2kΩ, R_{IN} = 110Ω, C_{IN} = 10pF

$$f_{-3dB} = \frac{1}{2\pi (110)\ 10 \cdot 10^{-12}} = 145MHz$$

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascade input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 60Ω then the total input capacitance, C_{IN} = (1+7.5) pF which will lead to only a 12% bandwidth reduction.

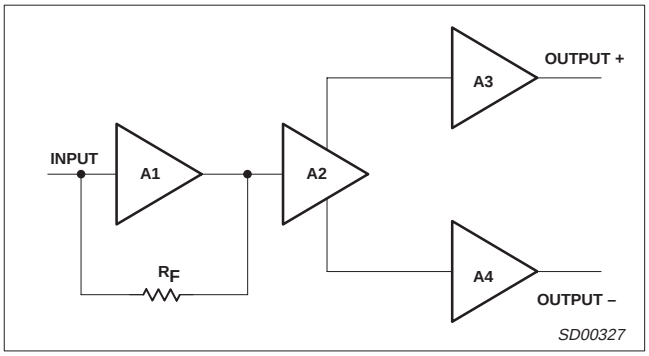


Figure 10. SA5212A – Block Diagram

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/√Hz. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 52nA RMS in a 200MHz bandwidth.

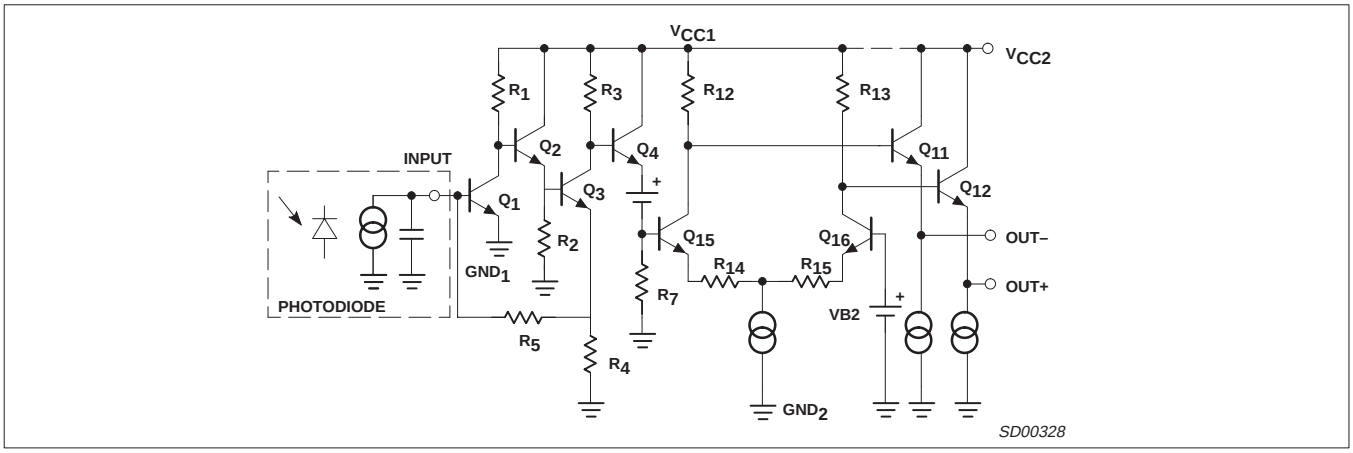


Figure 11. Transimpedance Amplifier

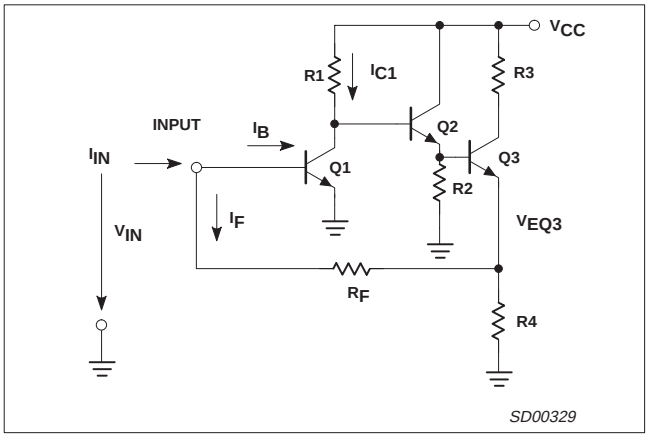


Figure 12. Shunt-Series Input Stage

DYNAMIC RANGE

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 120µA and a wideband noise of I_{EQ}=52nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = \frac{\text{(Max. input current)}}{\text{(Peak noise current)}}$$

$$D_E(\text{dB}) = 20\log\frac{(120 \cdot 10^{-6})}{(\sqrt{2}\ 52\text{nA})}$$

$$D_E(\text{dB}) = 20\log\frac{(120\mu\text{A})}{(73\text{nA})} = 64\text{dB}$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one Photon = $\frac{hc}{\lambda}$ watt sec (Joule)

Where h=Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^8 m/sec

c / λ = optical frequency

No. of incident photons/sec= where P=optical incident power

No. of incident photons/sec = $\frac{P}{\frac{hc}{\lambda}}$

where P = optical incident power

No. of generated electrons/sec = $\eta \cdot \frac{P}{\frac{hc}{\lambda}}$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole paris}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{P}{\frac{hc}{\lambda}} \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

Responsivity R = $\frac{\eta \cdot e}{\frac{hc}{\lambda}}$ Amp/watt

$$I = P \cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B=200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{52 \cdot 10^{-9}}{(1.6 \cdot 10^{-19})(200 \cdot 10^6)} = 1625\left(\frac{\text{Amp}}{\text{Amp}}\right)$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\lambda}B\ Z = 12\ (2.3 \cdot 10^{-19})$$

$$200 \cdot 10^6\ 1625 = 897\text{nW} = -30.5\text{dBm},$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the SA5212A, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{897 \cdot 10^{-9} \cdot 1.6 \cdot 10^{-19}}{2.3 \cdot 10^{-19}}$$

$$= 624\text{nA}$$

Choosing the maximum peak overload current of I_{avMAX}=120μA, the maximum mean optical power is:

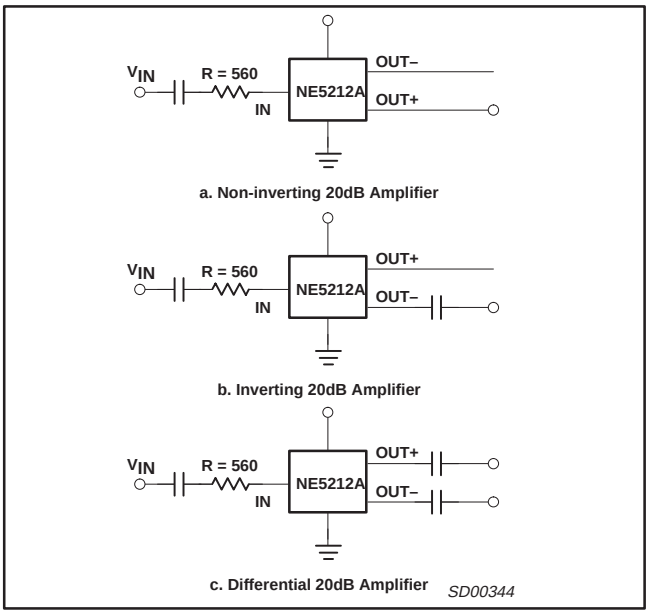


Figure 13. Variable Gain Circuit

$$P_{avMAX} = \frac{hcI_{avMAX}}{\lambda q} = \frac{2.3 \cdot 10^{-19}(120 \cdot 10^{-6})}{1.6 \cdot 10^{-19}}$$

$$= 172\mu W \text{ or } -7.6dBm$$

Thus the optical dynamic range, D_O is:

$D_O = P_{avMAX} - P_{avMIN} = -30.5 - (-7.6) = 22.8dB$.

This represents the maximum limit attainable with the SA5212A operating at 200MHz bandwidth, with a half mark/half space digital transmission at 820nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the SA5212A has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

BASIC CONFIGURATION

A trans resistance amplifier is a current-to-voltage converter. The forward transfer function then is defined as voltage out divided by current in, and is stated in ohms. The lower the source resistance, the higher the gain. The SA5212A has a differential transresistance of 14kΩ typically and a single-ended transresistance of 7kΩ typically. The device has two outputs: inverting and non-inverting. The output
voltage in the differential output mode is twice that of the output voltage in the single-ended mode. Although the device can be used without coupling capacitors, more care is required to avoid upsetting the internal bias nodes of the device. Figure 13 shows some basic configurations.

VARIABLE GAIN

Figure 14 shows a variable gain circuit using the SA5212A and the SA5230 low voltage op amp. This op amp is configured in a non-inverting gain of five. The output drives the gate of the SD210 DMOS FET. The series resistance of the FET changes with this output voltage which in turn changes the gain of the SA5212A. This circuit has a distortion of less than 1% and a 25dB range, from -42.2dBm to -15.9dBm at 50MHz, and a 45dB range, from -60dBm to -14.9dBm at 10MHz with 0 to 1V of control voltage at V_{CC}.

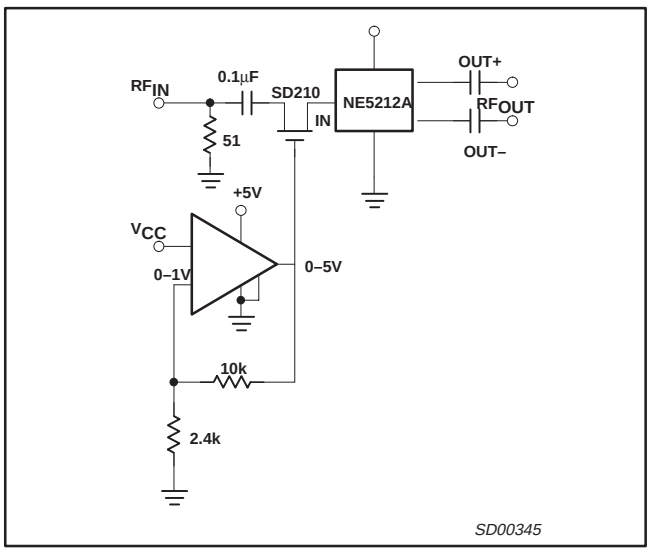


Figure 14. Variable Gain Circuit

16MHZ CRYSTAL OSCILLATOR

Figure 15 shows a 16MHz crystal oscillator operating in the series resonant mode using the SA5212A. The non-inverting input is fed back to the input of the SA5212A in series with a 2pF capacitor. The output is taken from the inverting output.

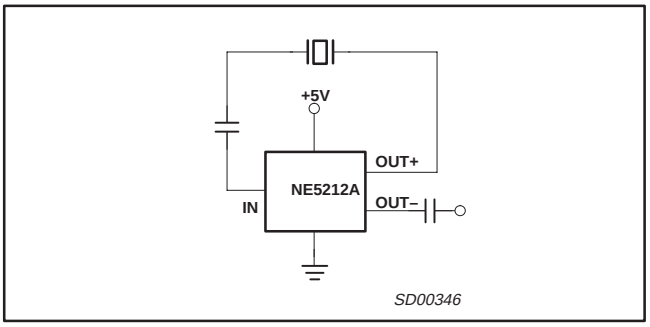


Figure 15. 16MHz Crystal Oscillator

DIGITAL FIBER OPTIC RECEIVER

Figures 16 and 17 show a fiber optic receiver using off-the-shelf components.

The receiver shown in Figure 16 uses the SA5212A, the Philips Semiconductors 10116 ECL line receiver, and Philips/Amperex BPF31 PIN diode. The circuit is a capacitor-coupled receiver and utilizes positive feedback in the last stage to provide the hysteresis. The amount of hysteresis can be tailored to the individual application by changing the values of the feedback resistors to maintain the desired balance between noise immunity and sensitivity. At room temperature, the circuit operates at 50Mbaud with a BER of 10E-10 and over the automotive temperature range at 40Mbaud with a BER of 10E-9. Higher speed experimental diodes have been used to operate this circuit at 220Mbaud with a BER of 10E-10.

Figure 17 depicts a TTL receiver using the SA5212A and the SA5214 fast amplifier system along with the Philips/Amperex PIN diode. The system shown is optimized for 50 Mb/s Non Return to Zero (NRZ) data. A link status indication is provided along with a jamming function when the input level is below a user-programmable threshold level.

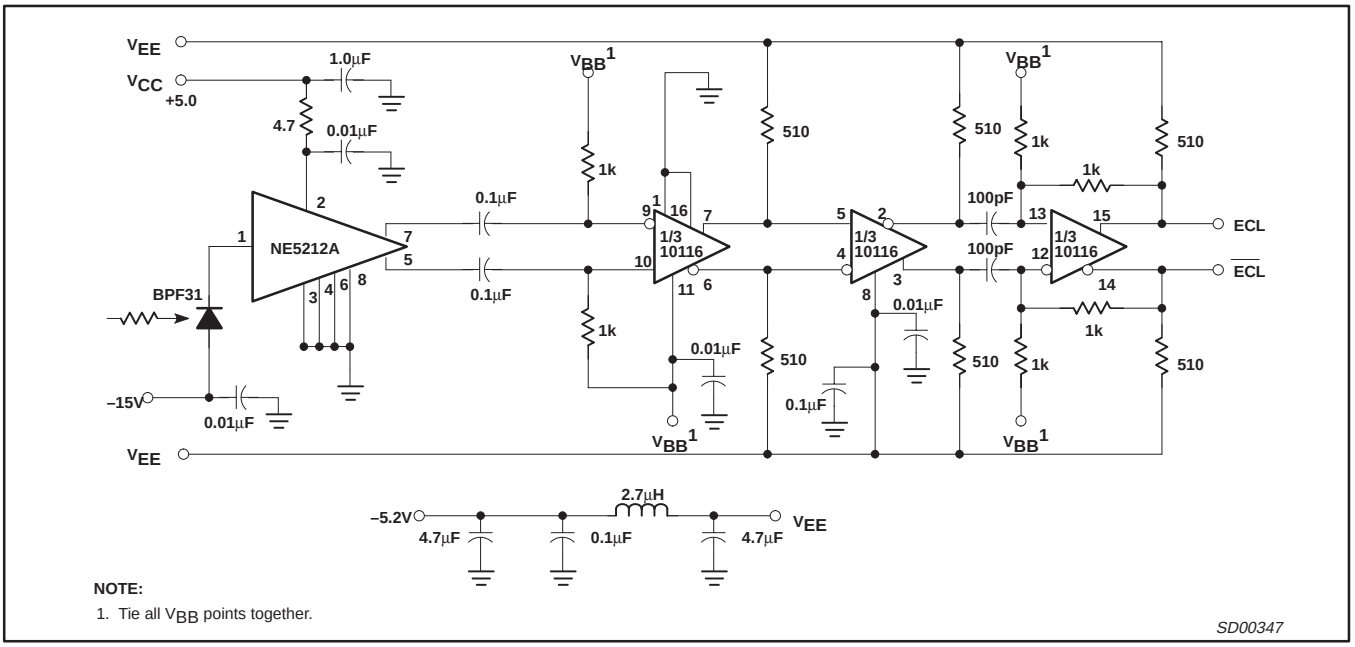


Figure 16. ECL Fiber Optic Receiver

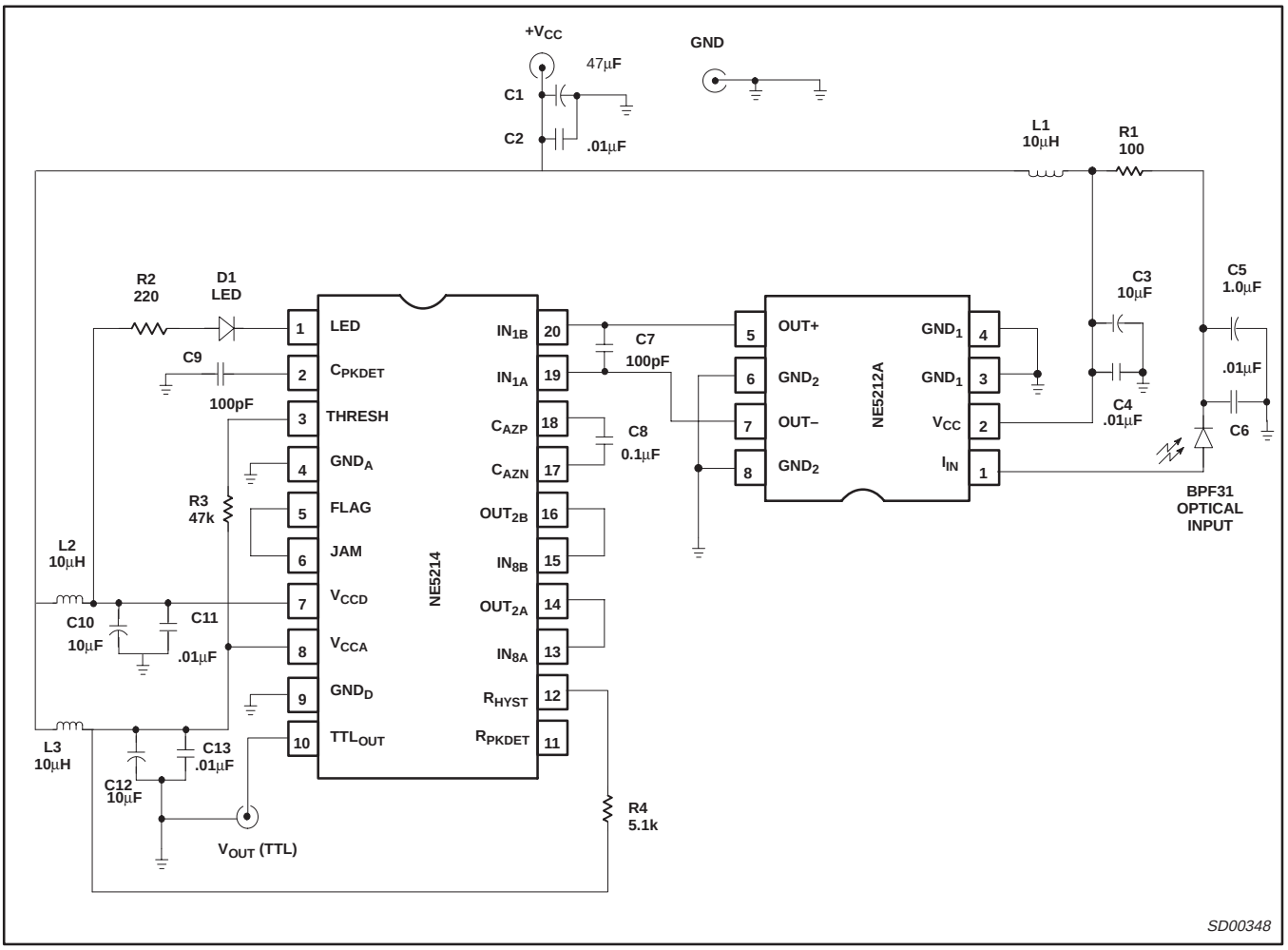


Figure 17. A 50Mb/s TTL Digital Fiber Optic Receiver

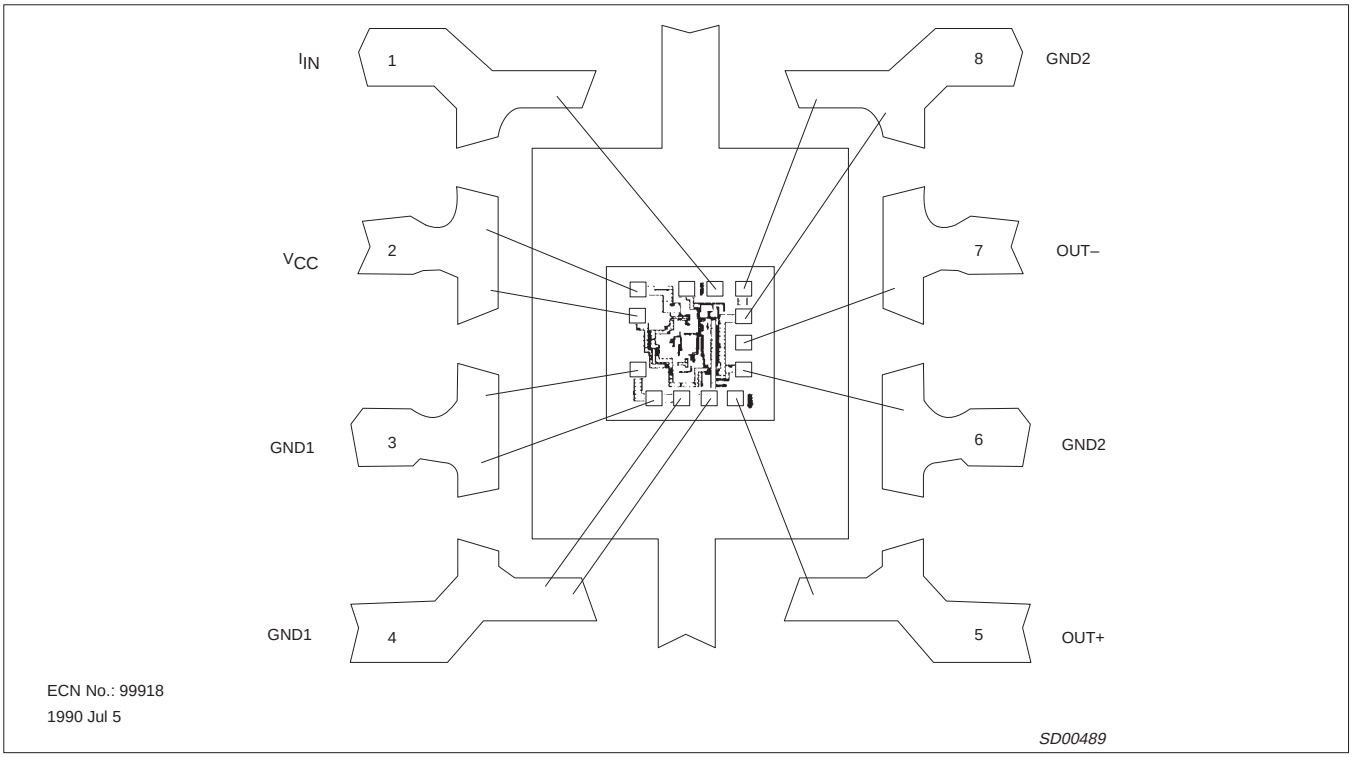


Figure 18. SA5212A Bonding Diagram

Die Sales Disclaimer

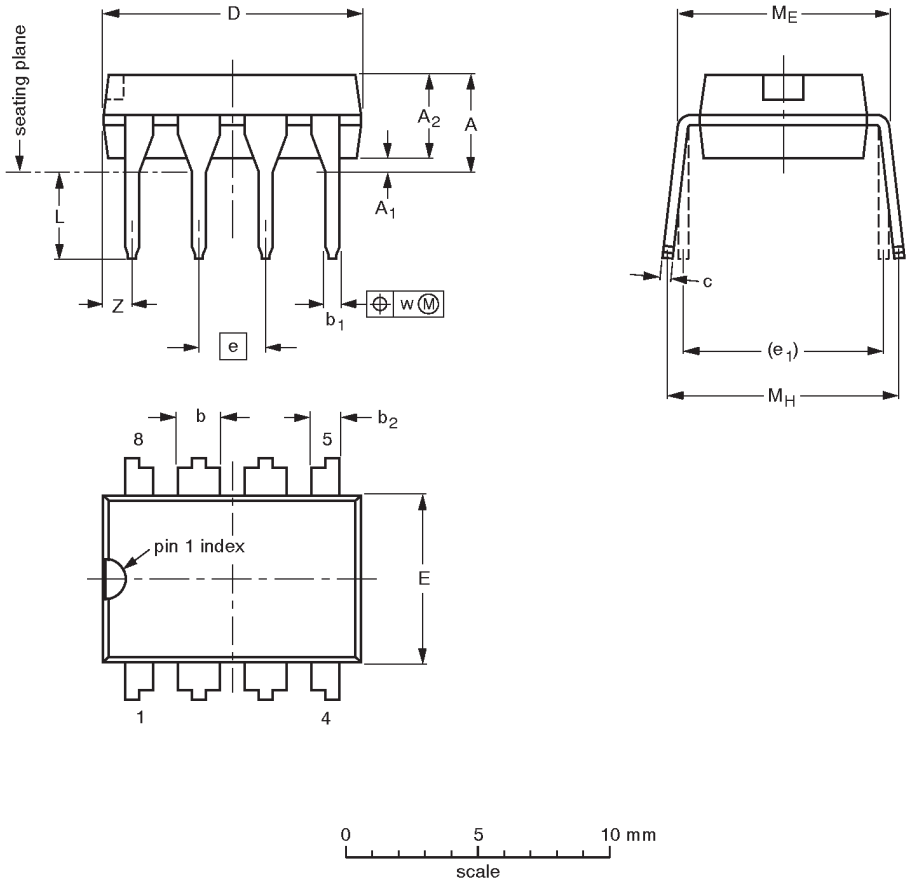
Due to the limitations in testing high frequency and other parameters at the die level, and the fact that die electrical characteristics may shift after packaging, die electrical parameters are not specified and die are not guaranteed to meet electrical characteristics (including temperature range) as noted in this data sheet which is intended only to specify electrical characteristics for a packaged device.

All die are 100% functional with various parametrics tested at the wafer level, at room temperature only (25°C), and are guaranteed to be 100% functional as a result of electrical testing to the point of wafer sawing only. Although the most modern processes are utilized for wafer sawing and die pick and place into waffle pack carriers, it is impossible to guarantee 100% functionality through this process. There is no post waffle pack testing performed on individual die.

Since Philips Semiconductors has no control of third party procedures in the handling or packaging of die, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems on any die sales.

Although Philips Semiconductors typically realizes a yield of 85% after assembling die into their respective packages, with care customers should achieve a similar yield. However, for the reasons stated above, Philips Semiconductors cannot guarantee this or any other yield on any die sales.

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

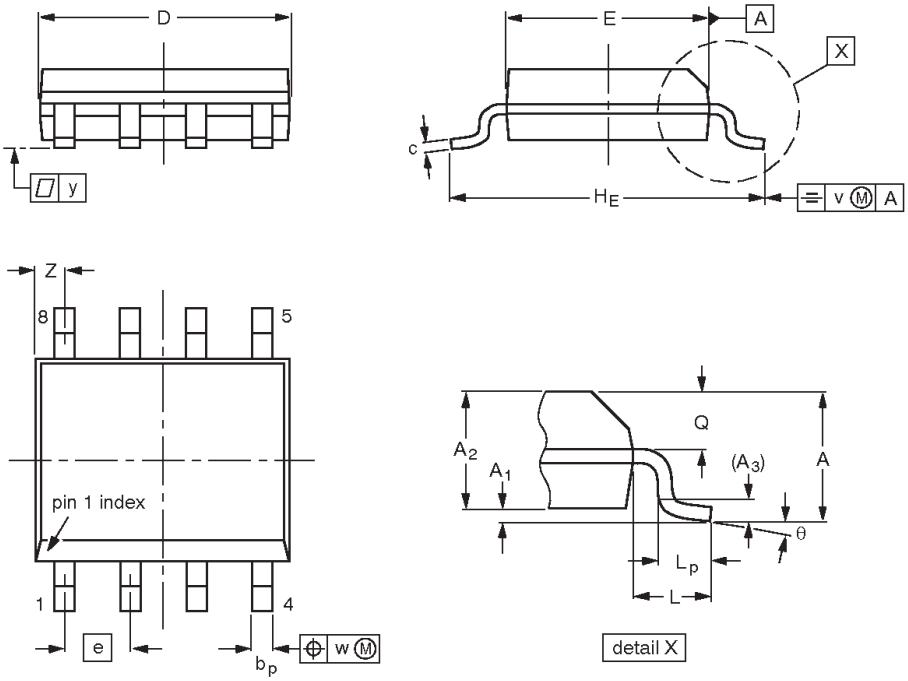
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

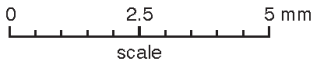
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 3.9mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

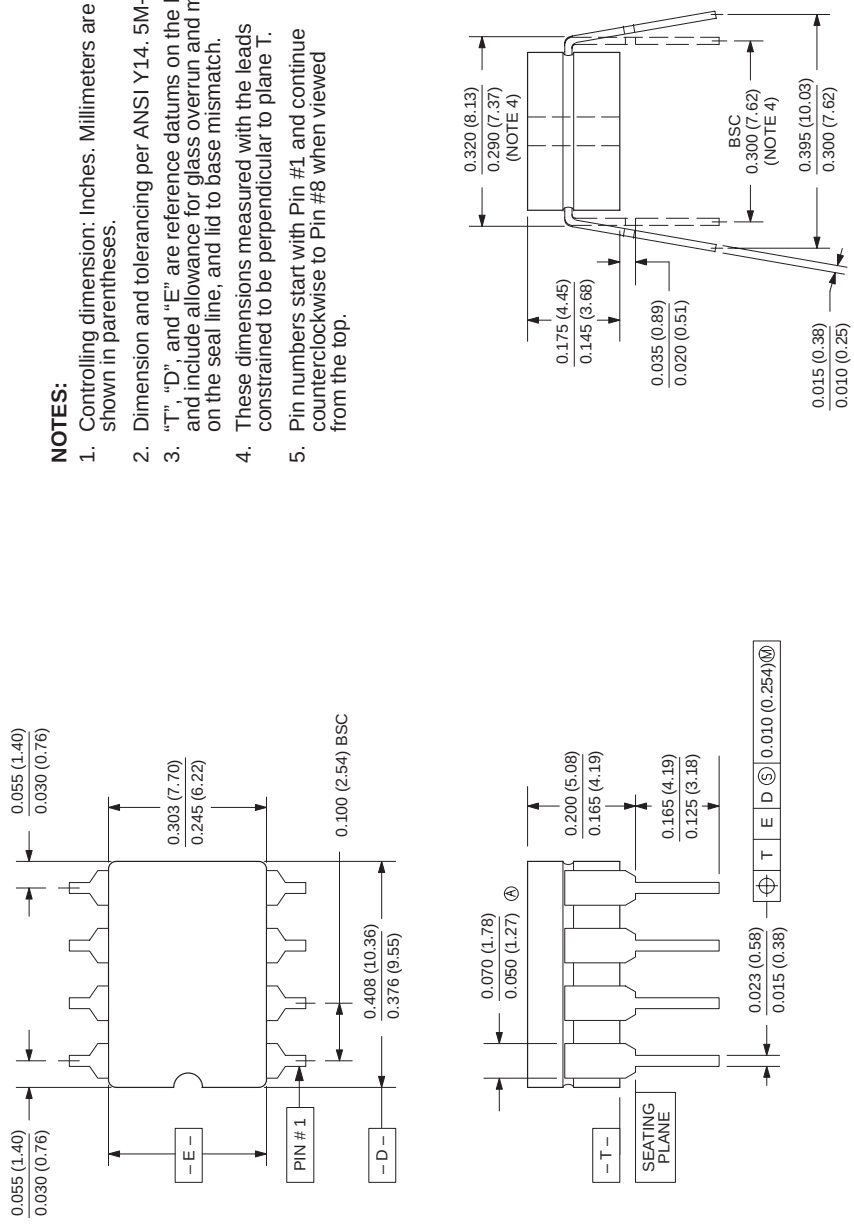
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

0580A 8-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE



Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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